

PREVIEW



CLICK HERE TO
DOWNLOAD
THE FULL
BOOK

MKS HANDBOOK



Process Technologies
in Advanced Packaging
by the Office of the CTO



PREVIEW

CLICK HERE TO
DOWNLOAD
THE FULL
BOOK

MKS Handbook

Process Technologies in Advanced Packaging

by the Office of the CTO

Dive deep into the Future of **Semiconductor Integration** and explore the engineering behind **Advanced Packaging** – the key to sustaining Moore’s Law in the post-scaling era.

As traditional transistor scaling approaches its physical limits, the semiconductor industry is turning to Advanced Packaging to maintain performance growth. This paradigm shift enables the integration of multiple heterogeneous dies into a single package, unlocking new levels of functionality, bandwidth, and power efficiency.

Our **Process Technologies in Advanced Packaging Handbook** is a comprehensive technical resource for anyone who wants to understand the next frontier in semiconductor design and manufacturing.

What you’ll gain from this handbook:

- A foundational understanding of heterogeneous integration and chiplet architectures
- Detailed insights into interposer technologies, through-silicon vias (TSVs), RDLs, and high-density interconnects
- Process flows and equipment used in 2.5D/3D packaging, fan-out wafer-level packaging (FOWLP), and system-in-package (SiP) solutions
- Whether you're designing next-gen systems or studying semiconductor fabrication, this handbook will equip you with the technical depth to innovate in a rapidly evolving landscape.

Download the complete Handbook and get hands-on with the technologies shaping the future of electronics.

PREVIEW

CLICK HERE TO
DOWNLOAD
THE FULL
BOOK

5/2025
© 2025 MKS Inc.
All rights reserved.

Limit of Liability/Disclaimer of Warranty: The purpose of this book is to educate and should be used only as a general guide. The authors and publisher are providing this book and its contents on an "as is" basis and make no representations or warranties of any kind. Neither the authors nor the publisher shall be liable for any costs, damages and expenses whatsoever (including, without limitation, incidental, special and consequential damages) resulting from any use of or reliance on the information contained herein, whether based on warranty, contract, tort or any other legal theory, and whether or not they have been advised of the possibility of such damages.

This document shall not be copied, reproduced, distributed or published, in whole or in part, without the prior written consent of MKS Inc.

ASF®, Aurotech®, BondFilm®, Coppertreat®, CupraEtch®, Cupraganth®, CupraPro®, EcoFlash®, G-Plate®, Innolyte®, InPro®, Inpulse®, MultiPlate®, Neoganth®, NovaBond®, OS-Tech®, Oxamat®, PallaBond®, PallaStrip®, PD-Core®, ProSelect®, ResistStrip®, Securiganth®, Solderbond®, Spherolyte®, Stannatech®, Stanna-CAT®, Uniplate®, vPlate®, Xenolyte® are registered trademarks of MKS Inc. or a subsidiary of MKS Inc. All other trademarks cited herein are the property of their respective owners.



Foreword

Semiconductor devices are essential and ubiquitous parts of our lives, enabling everything from artificial intelligence (AI) to autonomous vehicles to wireless networks. Driven by Moore's Law, which states that the number of transistors on a microchip doubles approximately every two years, the industry has pursued a relentless reduction in cost per function for the better part of a century. Historically, the industry used Dennard scaling and multi-core architectures to achieve these results. However, traditional transistor scaling has slowed, but the need to continue reducing cost per function at the same historical pace is paramount; otherwise, new innovations will become cost prohibitive.

The latest technological evolution introduced to overcome this limitation is called heterogeneous packaging, often referred to as Advanced Packaging. Traditional packaging involves packaging a single semiconductor chip, while Advanced Packaging integrates multiple specialized chips into a single package, allowing them to function as a single chip. This enables continued performance gains for electronic devices, despite the slowdown of traditional transistor scaling.

Advanced Packaging encompasses a wide variety of architectures and process technologies, enabling a modular approach to integrating more semiconductor devices with ever greater IO (Input/Output) density. It has become essential for various modern microelectronic applications, including AI and High-Performance Computing servers that require raw compute power with integrated high bandwidth memory and mobile devices that demand specific size, weight, and power requirements. These needs continue to drive its development. Advanced Packaging is a key innovation, often referred to as "More than Moore's Law," helping to keep the industry on the trajectory predicted by Moore's Law.

Integral to this packaging are interconnect process technologies. MKS has strategically expanded its portfolio of foundational solutions, acquiring Electro Scientific Industries, a leader in laser via drilling systems, in 2019, and Atotech, a critical provider of specialty chemistry solutions to uniquely enable next-generation interconnect formation, in 2022. The combination of these capabilities within MKS enables an accelerated time-to-market with a turn-key solution comprising MKS' Optimize the Interconnect® offering.

The purpose of this Handbook is to introduce the reader to the basics of Semiconductor Advanced Packaging and its process technologies, as well as the key products and applications that Optimize the Interconnect. As with our first two Handbooks, *MKS Instruments Handbook of Semiconductor Devices and Process Technology, 2nd Edition* and *MKS Instruments Handbook of Principles and Applications in Photonics Technologies*, we've learned from working alongside you for many decades and we hope you find this Handbook informative and useful. We welcome your feedback and input for future editions. Rapidly evolving technology will continue to shape and transform this industry in the years to come. MKS looks forward to addressing the opportunities and challenges this will present – together.

John T.C. Lee
President & Chief Executive Officer



About MKS Inc.

MKS Inc. enables technologies that transform our world. We deliver foundational technology solutions to leading edge semiconductor manufacturing, electronics and packaging, and specialty industrial applications. We apply our broad science and engineering capabilities to create instruments, subsystems, systems, process control solutions and specialty chemicals technology that improve process performance, optimize productivity and enable unique innovations for many of the world's leading technology and industrial companies. Our solutions are critical to addressing the challenges of miniaturization and complexity in advanced device manufacturing by enabling increased power, speed, feature enhancement, and optimized connectivity. Our solutions are also critical to addressing ever-increasing performance requirements across a wide array of specialty industrial applications. Additional information can be found at www.mks.com.



Table of Contents

[CLICK HERE TO
DOWNLOAD
THE FULL
BOOK](#)

Chapter 1 - Semiconductor Packaging
1.1 Introduction.....
1.1.1 Design and Manufacturing.....
1.1.2 Applications and Future Trends.....
1.1.3 Book Overview	06
1.2 Semiconductor Package Design	07
1.2.1 Semiconductor Packaging Substrates.....	08
1.3 Evolution in Packaging Architecture	13
1.4 System-in-Package (SiP)	15
1.4.1 SiP Modules.....	15
1.5 PCB and IC Substrate Fabrication and Packaging.....	18
1.6 Technology Roadmaps	21
References.....	24
Chapter 2 - Packaging Architecture, Interposers, and Interconnect Technologies	26
2.1 Introduction.....	28
2.2 Packaging Architecture	29
2.2.1 2D Architecture.....	29
2.2.2 Enhanced Architectures.....	29
2.2.3 2D/3D Architectures - Classification and Nomenclature.....	30
2.3 Interposer Types.....	32
2.3.1 2D Leadframes	32
2.3.2 2.1D Organic Interposers	40
2.3.3 2.3D Organic Interposers	40
2.3.4 2.5D Organic Interposer - Special Form- Embedded Die (Si Bridges, EMIB).....	41
2.3.5 2.5D Silicon Interposers - TSV (Passive and Active Solutions).....	44
2.3.6 2.5D Glass Interposer - TGV	46
2.3.7 3D Interposer Architecture.....	48
2.4 Interconnect Technologies.....	49
2.4.1 Wirebond.....	51
2.4.2 Flip Chip, Solder Balls and C4 Bumps.....	53
2.4.3 Redistribution Layers, RDLs.....	54
2.4.4 Microbumps.....	56



2.4.5 Tall Pillar (Pre-formed Through Package Vertical Contacts/Vias (TPV)).....58
2.4.6 Through Silicon Vias (TSV)59
2.4.7 Direct Bonding61
2.4.8 Thermal Compression Bonding.....61
2.4.9 Hybrid Bonding.....62
2.4.10 Wafer-to-Wafer (W2W) vs. Die-to-Wafer (D2W) Interconnect Formation63
References.....64

Chapter 3 - Organic Laminate Structure..... 68

3.1 Introduction to Common Formats and Materials.....70
3.1.1 Copper Foils71
3.1.2 Resin and Woven Glass Fabric.....72
3.1.3 Prepreg and Copper Clad Laminate (CCL).....73
3.2 Semi-Additive Process and Build-Up Films76
3.3 Solder Masks81
3.4 Process Flows84
3.4.1 High Density Interconnect Technology84
3.4.2 Semi-Additive Processes (SAP).....84
3.4.3 Embedded Structures86
References.....92

Chapter 4 - IC Substrate Manufacturing Process Technologies/Equipment 93

4.1 Introduction.....95
4.2 Substrate Core96
4.2.1 Overview96
4.2.2 Base Materials96
4.2.3 Substrate Fabrication Processes.....97
4.2.4 Glass Core Substrate (GCS)98
4.3 Lamination.....99
4.4 Via Drilling.....101
4.4.1 Introduction.....101
4.4.2 Via Drilling for Glass-reinforced Copper-clad Laminate (CCL)101
4.4.3 Laser Drilling of Ajinomoto Build-up Film (ABF).....106
4.4.4 Additional Materials of Interest: RCC and GCP107
4.4.5 MKS Products for Laser Drilling.....107



4.5	Metallization: Desmear and Electroless Copper.....	110
4.5.1	Desmear.....	110
4.5.2	MKS Products for Desmear.....	111
4.5.3	Surface Activation and Patterning.....	112
4.5.4	MKS Products for Surface Activation.....	113
4.5.5	Electroless Copper Deposition.....	114
4.5.6	MKS Products for Electroless Copper Deposition.....	115
4.5.7	Electroless Copper and Joint Reliability.....	116
4.5.8	MKS Production Equipment.....	118
4.6	Patterning.....	121
4.6.1	Overview.....	121
4.6.2	Dry Film Photoresist and Projection Photolithography.....	121
4.6.3	Mask/Stepper Based Patterning.....	122
4.6.4	Maskless Patterning.....	122
4.7	Electrochemical Deposition of Metals.....	124
4.7.1	Electroplating Pre-Treatment.....	125
4.7.2	MKS Products for Electroplating Pre-treatment.....	126
4.7.3	Direct Current vs. Reverse Pulse Plating.....	126
4.7.4	Copper Filling of Blind Micro Vias.....	128
4.7.5	MKS Products for Blind Micro Via Filling.....	131
4.7.6	Through Via Filling.....	131
4.7.7	MKS Products for Through Via Filling.....	132
4.7.8	High Hole Density (conformal) - Reverse Pulse.....	133
4.7.9	Pillar Plating.....	134
4.7.10	MKS Products for Pillar Plating.....	136
4.7.11	ECD Cu – Physical Properties and Reliability.....	136
4.7.12	Thickness Uniformity.....	138
4.7.13	Plating Equipment.....	139
4.7.14	MKS Uniplate® Cu Plater.....	141
4.7.15	MKS Products for Uniplate® Cu Plater.....	144
4.7.16	MKS vPlate® Vertical Conveyorized Plating Tools.....	145
4.7.17	MKS Products for vPlate® VCP Plater.....	146
4.7.18	Single Panel Tools.....	146
4.7.19	MKS Products for MultiPlate® Single Panel Tool.....	146



- 4.8 Circuitization..... 147
 - 4.8.1 Dry Film Pre-treatment 147
 - 4.8.2 MKS Products for Dry Film Pre-treatment 147
 - 4.8.3 Dry Film Removal 148
 - 4.8.4 MKS Products for Dry Film Removal..... 148
 - 4.8.5 Copper Seed Layer and Palladium Removal..... 149
 - 4.8.6 MKS Products for Copper Seed Layer and Palladium Removal 150
 - 4.8.7 Bonding..... 151
 - 4.8.8 MKS Products for Bonding..... 151
- 4.9 Final Finishing 154
 - 4.9.1 Why is a Final Finish Needed..... 154
 - 4.9.2 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) 155
 - 4.9.3 Electroless Nickel/Immersion Gold (ENIG) 156
 - 4.9.4 Nickel-free Precious Metal Finishes: Electroless Palladium/Autocatalytic Gold (EPAG), Gold/Palladium/Gold, Direct Immersion Gold (DIG) 157
 - 4.9.5 Organic Solder Protection (OSP)..... 158
 - 4.9.6 Immersion Tin (ISn) 159
 - 4.9.7 Horizontal Immersion Tin Equipment..... 160
 - 4.9.8 Requirements for Final Finishes in the Package Substrate Industry..... 162
 - 4.9.9 Second Image Technology 166
- References..... 167

Chapter 5 - Flip Chip Packaging and Assembly 170

- 5.1 Introduction..... 172
- 5.2 Major Parameters Advantages and Disadvantages of Flip Chip..... 174
 - 5.2.1 Parameters 174
 - 5.2.2 Advantages and Disadvantages 176
- 5.3 Variants of Flip Chip Packages..... 178
 - 5.3.1 Flip Chip CSP..... 178
 - 5.3.2 Flip Chip Ball Grid Array and Pin Grid Array 178
 - 5.3.3 High Performance Flip Chip BGA (HFCBGA)..... 180
 - 5.3.4 Applications [2] 180
 - 5.3.5 Features [2] 180
 - 5.3.6 Process Flow and Variants 180
 - 5.3.7 MKS C4 and Microbump Products (also see Chapter 2.4.4)..... 182
- 5.4 UBM and Solder Bumping 183



5.4.1 Evaporation Vacuum Reflow Bonding..... 184

5.4.2 Electroplating Technique..... 185

5.4.3 MKS RDL Products..... 185

5.4.4 Printing Technique..... 185

5.4.5 Special Forms of Solder Bumping: Stud Bumping and Laser Assisted Bonding 186

5.5 Flip Chip Bonding – The FC Assembly Process 187

5.5.1 Thermocompression and Thermosonic Bonding 190

5.5.2 Bonding with Isotropic and Anisotropic Adhesives..... 191

5.5.3 Flip Chip Underfill 191

5.5.4 Emerging Technologies for Flip Chip Assembly..... 193

5.5.5 MKS Products (also see Chapter 2.4.9)..... 193

5.6 Encapsulation, Molded Underfill and Solder Ball Attach 194

5.6.1 Encapsulation with Molded Underfill 195

5.6.2 Solder Ball Attach for BGA Package..... 196

5.7 Flip Chip Package Singulation 197

5.8 Marking, Inspection, Electrical Test, and Packing..... 198

References..... 199

Chapter 6 - Wafer Level Packaging 200

6.1 Introduction 202

6.2 Fan-In Wafer Level Packaging (WLP)..... 204

6.3 Fan-Out Wafer Level Packaging..... 207

6.3.1 FOWLP Technologies and Platforms..... 210

6.3.2 Chip-first Face-down Technology 211

6.3.3 Chip-first Face-up Technology 212

6.3.4 Chip-last Technology (RDL-first) – “Advanced Flip Chip” Process Encapsulation..... 213

6.3.5 Backside RDL..... 214

6.4 Fan-Out Panel Level Packaging (FOPLP)..... 215

6.4.1 Technologies, Materials, and Equipment used for PLP and WLP Technology..... 217

6.4.2 Reliability Testing of FOPLP 222

6.5 MKS Product Solutions..... 223

6.5.1 ECD Equipment: Multiplate® and G-Plate® (WLP and PLP) 223

6.5.2 ECD Chemicals: Spherolyte® Cu UF2/UF3, Spherolyte® Ni, and Spherolyte® SnAg 223

References..... 225



Chapter 7 - Integration in Packaging..... 227

- 7.1 Monolithic Integration (System-on-Chip)..... 229
- 7.2 Die Stacking 230
 - 7.2.1 3D IC Packaging and 3D IC Integration..... 230
 - 7.2.2 3D IC Packaging..... 230
 - 7.2.3 3D IC Integration..... 232
- 7.3 System in Package..... 233
- 7.4 Package on Package..... 237
- 7.5 Heterogenous Integration 239
- 7.6 Chiplets.....244
- 7.7 MKS Products..... 246
- References.....247

Glossary.....248



PREVIEW

**CLICK HERE TO
DOWNLOAD
THE FULL
BOOK**

Chapter 1

Semiconductor Packaging



1.1 Introduction

A semiconductor package (component level/level 1) is the enclosure of one or more integrated circuit (IC) dies and serves as a bridge between the IC (chip level/level 0) and the next assembly level (board level/level 2), allowing for easy integration into electronic applications and systems (system level/level 3).

Figure 1 illustrates the main purposes of a package [1,2]:

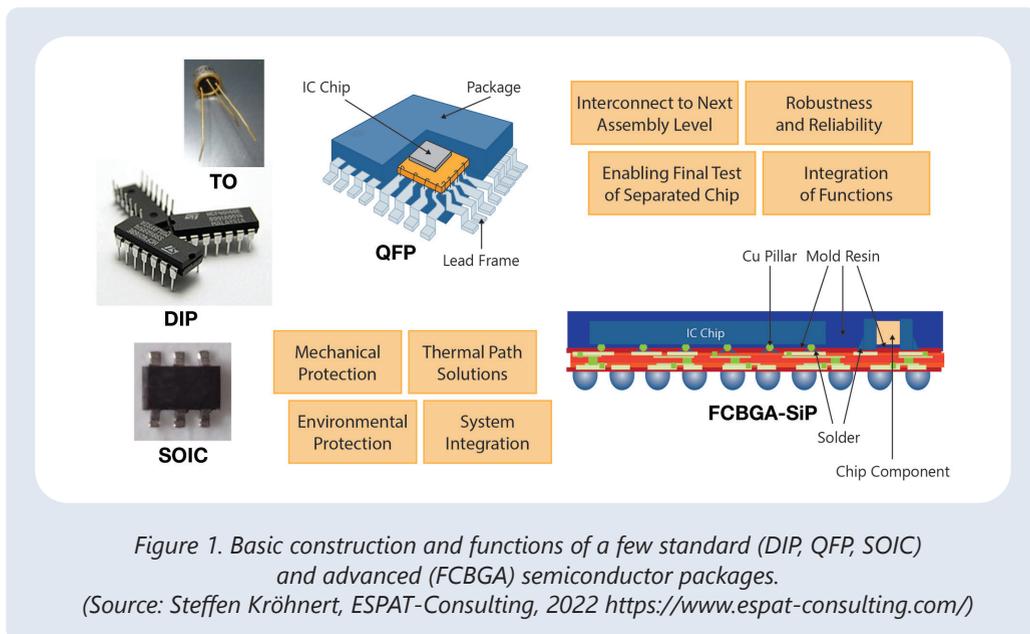
Interconnect to the Next Assembly Level: The package facilitates electrical interconnection between the die and the external circuitry at the next assembly level, enabling the flow of electrical signals and power.

Environmental Protection and Mechanical Support: The package shields the semiconductor die from thermal, environmental stresses, and electrostatic discharge. It also provides structural support for the chip, ensuring it remains securely attached to the substrate or circuit board, improving its robustness, reliability, and lifespan.

Thermal Path Solutions: Semiconductor devices generate heat during operation and the package must facilitate thermal transfer to dissipate the heat. Packages often incorporate heat sinks, thermal pads, or other thermal transport solutions that prevent overheating and allow the IC to function optimally, even in high-temperature environments.

Test and System Integration: The package facilitates the integration of the chip into more complex electronic devices, allowing for easier handling and assembly at the next level of manufacturing as well as electrical testing.

Since the advent of semiconductor packaging technology in the 1950s, several thousand package types have evolved with two major trends standing out: the desire for ever higher input/output (I/O) channels and achieving the smallest possible device footprint. Early semiconductor devices were packaged using 'Transistor Outline' (TO) metal cans (Figure 1) or ceramic packages and simple wire bonding for electrical connections. As the industry evolved, there was a need for smaller, more reliable,





and cost-effective packaging solutions. This led to the development of Dual In-line Packages (DIPs), which came to volume production in the 1970s. As shown in Figure 1, DIPs had a rectangular body with two parallel rows of pins that could be directly plugged into sockets on circuit boards. Later in the 1970s, Plastic Quad Flat Packages (PQFPs) with a plastic body replaced traditional ceramic packages. These had a smaller form factor, a lower cost and better manufacturability and could be surface mounted on printed circuit boards (PCBs). Also, PQFPs improved thermal and electrical performance. Further advances in surface mount technology (SMT) led to the development of small-outline integrated circuit (SOIC) packages with smaller footprints and improved thermal characteristics compared to DIPs.

Semiconductor dies became larger in the 1980s and 1990s, driven by the increasing functionality and I/O count needed for computing, networking, and storage application requirements. Chips with 1 million transistors were introduced [1], and packaging technology had to evolve to accommodate the significant increases in the number of I/O counts. Pin Grid Arrays (PGA) and Ball Grid Arrays (BGA) (Figure 6) became significant packaging modes. These featured an array of solder balls on the underside of the package that provided the electrical connections to the PCB. Such grid arrays improved electrical performance, reduced inductance, and enhanced thermal management, making them suitable for high-speed and high-density applications. In the 90s, the Chip Scale Package (CSP) was introduced to address even higher pin counts within a very compact size requirement. Wafer-Level Packaging (WLP) which provides the electrical connections and encapsulation of semiconductor chips before singulation, i.e. 'at the wafer level' gained traction in the 2000s. WLP introduced technologies such as Redistribution Layers (RDL) and Through Silicon Vias (TSVs) that enhanced interconnectivity and 3D integration. These marked the beginnings of what today is called 'Advanced Packaging'. As with most technologies, standard or 'traditional' packaging is not going anywhere but continues to be applied at scale for products where cost-effectiveness, reliability, and ease of manufacturing are the primary considerations. [2]

As the design costs of the most advanced semiconductor nodes increased exponentially and high yields for ever larger size chips at these advanced nodes became ever more challenging to maintain in the pursuit of maintaining Moore's Law, a 'new' approach gained traction as an attractive alternative which Gordon Moore already anticipated in 1965 [10]: "It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected." Where monolithic, traditional chips provide all functionalities on a single silicon die necessarily manufactured at the most advanced process technology node needed for its highest performing aspect, chiplets break down the capabilities of a chip into smaller, modular dies that have a reduced or singular function and are designed to communicate with each other [13]. This allows for heterogeneous integration [12]: different chiplets are to be manufactured using different process nodes, different semiconductor materials, and even different manufacturers, appropriate for their specific function, which may go well beyond 'just' digital and can include RF communications, sensors, actuators, etc. This 'functional diversification' that goes beyond the shrinking of physical feature sizes of logic and memory is referred to as 'More than Moore' [20]. This modular approach enables easier scaling and upgrading as not all components need to be redesigned for every generation. In conjunction with the better yield of smaller individual die sizes and older process nodes for some of the chiplets, a more cost-effective and faster time to market has opened [5, 6, 7, BCG2024 "Advanced Packaging is Radically Reshaping the Chip Ecosystem"]. A corresponding 'Heterogeneous Integration Roadmap' was developed by IEEE in 2019 and is regularly updated. [3]

Advanced Packaging has emerged as the critical, enabling technology capable of connecting these smaller chips and chiplets next to and on top of each other in a wide variety of architectures for 2.XD and 3.XD packaging. These new architectures provide very high bandwidth through higher interconnect density and shorter connections in cost-effective, compact packages that leverage ever more sophisticated interconnect, interposer, and substrate technologies.



1.1.1 Design and Manufacturing

Modern package design requires careful modeling and simulation to ensure that these performance characteristics are met, taking the interplay of all components including the die, substrates, and interposers into account (Chapter 1.2). Package manufacturing involves several critical steps employing a broad swath of material and process technologies:

Die Preparation: The wafer is thinned to the required thickness, diced into individual dies, and then attached to the substrate or package.

Interconnect Formation: This step involves creating electrical connections between the die and the substrate. Techniques include horizontal, e.g., redistribution layers (RDL), as well as vertical interconnects, e.g., Through Silicon Vias (TSVs).

Encapsulation: The die and interconnects are encapsulated to protect them from environmental damage. This can be done using molding compounds or other encapsulation materials.

Substrate Attachment: The encapsulated die is attached to a substrate, which provides mechanical support and additional electrical connections.

More Interconnects: For certain packaging types, leadframes or solder bumps are formed to facilitate connections to the next level of assembly.

Testing and Inspection: The assembled package undergoes electrical testing and inspection to ensure functionality and reliability.

Marking and Packing: Finally, the packages are marked for identification and packed in trays, tape and reel, or other formats for shipment and integration into electronic devices.

1.1.2 Applications and Future Trends

Since their inception, smartphones and other mobile electronic devices have driven the integration of high-performance components into compact form factors using techniques like Fan-Out Wafer-Level Packaging (FOWLP) and System-in-Package (SiP). Advanced Packaging is essential for reliably and robustly connecting and integrating the manifold components, from Antenna-in-Package (AiP) systems that support higher frequencies for next-generation wireless communications (5G to 6G), to processors, memory, cameras, LiDAR, and other sensors.

Advanced Packaging has also become a key enabler for artificial intelligence (AI) and high-performance computing (HPC) as these applications require immense processing power harnessed across many interconnected chips, particularly to high bandwidth memory (HBM) (Figure 2), and efficient heat dissipation.

In the automotive sector, the shift towards autonomous and electric vehicles demands electronics that are not only powerful but also environmentally robust and reliable. Advanced Packaging ensures that these electronic components can withstand harsh conditions while maintaining high performance. Similarly, in the realm of biosensors and the Internet of Things (IoT), Advanced Packaging enables the integration of multiple functions into small, efficient packages, facilitating the development of compact and versatile devices.

Looking ahead, the future of Advanced Packaging is bright. According to a recent White House review [4], cited in [5] "...Advanced Packaging through heterogeneous integration will be critical as it... provides an alternative avenue for innovation in density and size of products." Moreover, "just as Moore's law led to the advancement of the global semiconductor industry over the past 55 years, heterogeneous integration is and will be the key technology direction going forward [6]."



Advanced Packaging has evolved into not just a complementary technology but a foundational one that supports the most advanced semiconductor technologies and is here to stay. Its role is critical in a world where electronic applications are ubiquitous and ever-expanding, ensuring that devices are more powerful, more efficient, and more reliable than ever before.

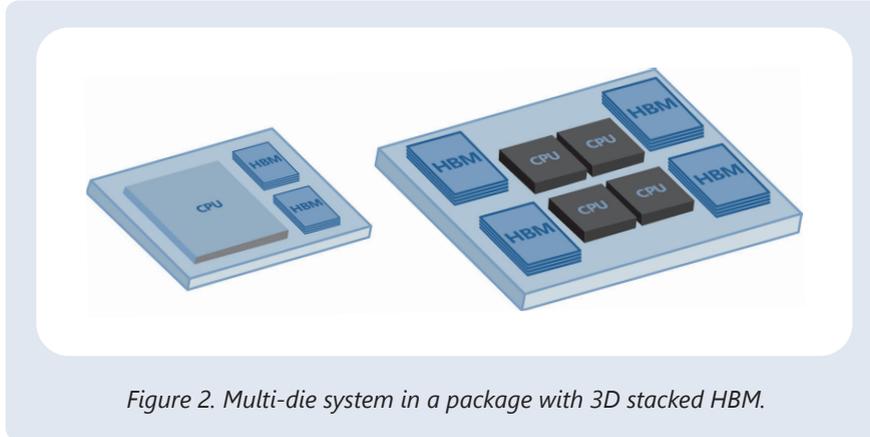


Figure 2. Multi-die system in a package with 3D stacked HBM.

1.1.3 Book Overview

The remainder of this handbook is structured as follows:

Chapter 1 provides a high-level overview of semiconductor package design and fabrication, as well as the associated roadmaps.

Chapter 2 covers packaging architectures and their nomenclature, interposer and interconnect technologies.

Chapter 3 discusses organic laminate IC substrates in terms of materials and process flows.

Chapter 4 goes into some detail exploring the process technologies necessary for IC substrate manufacturing, from the substrate core base materials and lamination, to via drilling, metallization and patterning, as well as metal deposition, circuitization, and final finishing.

Chapter 5 specifically addresses flip chip packaging and assembly in its various forms, their respective advantages and disadvantages, process flows and techniques, all the way to final marking, inspection, electrical test, and packaging.

Chapter 6 reviews wafer level packaging, both fan-in and fan-out in its various configurations, and its extension to panel level packaging.

Lastly, Chapter 7, presents the developments of integration in packaging from the monolithic System-on-Chip to System-on-Package, Package-on-Package, Heterogeneous Integration and Chipllets.

Throughout these Chapters, we point to specifically relevant MKS products in separately called out sections, except in cases where products are uniquely enabling process steps.



1.2 Semiconductor Package Design

While manufacturing technologies and designs may vary, all semiconductor packages must achieve certain minimal mechanical and environmental parameters:

Power Management, Efficiency, and Integrity: Energy consumption in electronic devices is currently doubling every three years and device efficiencies are not keeping pace [5]. In advanced devices, power losses during transmission and conversion must be minimized. Designs for power delivery networks need to manage high current densities while minimizing voltage drops and ensuring adequate power to each component. Furthermore, maintaining stable and precise voltage levels is challenging, especially when different components may have varying voltage requirements.

Signal Integrity (SI): Signal speed, noise sensitivity, and electromagnetic interference are becoming critical parameters due to the operating speeds of modern processors. Substrates that incorporate high speed interconnects are required to have a much lower dielectric constant than in the past. Noisy circuits can generate electromagnetic interference that can hamper the functionality of neighboring circuits. In some cases, interfering circuits may need to be separated from the other sensitive circuits by shielding the device or filtering the power and signal lines.

Heat Dissipation: The heat generated during circuit operation can impact the circuit's functionality and reliability, if not properly dissipated. Proper package design must provide a path for thermal transfer that maintains the IC junction temperatures below the threshold value. A package's ability to dissipate a chip's operational heat directly correlates with device reliability.

Modern packages must be optimized to minimize device size/weight, power consumption and cost (SWaP-C). Therefore, the design phase for electronic devices now employs next-generation Electronic Design Automation (EDA) software (Figure 3, Figure 4) that can incorporate all needed components and physical parameters to predict system behavior and cost. EDA simulations incorporate a comprehensive multi-scale sign-off approach that simulates physical phenomena such as power optimization, signal integrity, electrostatic discharge (ESD) effects, electromagnetic interference/electromagnetic compatibility (EMI/EMC), heat transfer, fluid dynamics and structural mechanics across chips, packages, and systems.

EDA software cannot, however, address all the design needs for multiple point tools/software, many of these have separate user interfaces and models, or are supported on different platforms that make data sharing almost impossible. A unified platform is needed that offers tight integration of system level signal, power, and thermal analysis while delivering automated power, thermal, and noise aware optimization. A consolidated view of the entire system is especially important since the power and thermal analysis of an individual die in isolation is no longer enough in a multi-die environment.

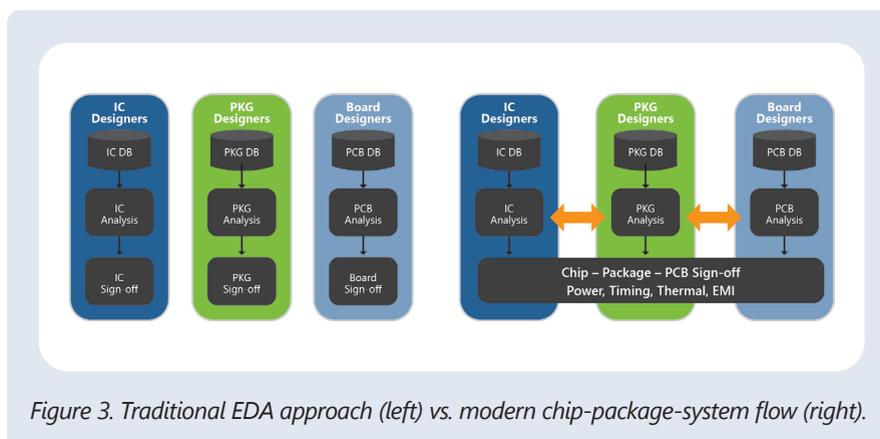


Figure 3. Traditional EDA approach (left) vs. modern chip-package-system flow (right).



1.2.1 Semiconductor Packaging Substrates

This discussion will focus on the classification of IC packages based on substrate type (Figure 4). The substrate serves as an intermediary that provides both mechanical support for the die and electrical connections to surrounding systems. This classification also includes two unique cases (i) where no substrate is used, and (ii) embedded die technology, which will be explored in this chapter. Three broad substrate classifications can be defined:

Organic Substrates: These are made of organic materials such as FR-4, which is a glass-reinforced epoxy laminate, or other polymer materials. Organic substrates are generally cost-effective and offer flexibility in design. They provide good electrical performance for a wide range of applications and are commonly used in consumer electronics.

Leadframe: A leadframe is a metal structure consisting of a central pad on which the die is placed surrounded by leads that connect the wiring from tiny electrical terminals on the semiconductor surface to the large-scale circuit connections on a circuit board (Figure 1). Leadframe substrates are typically low cost and offer excellent electrical and thermal performance. They have low design complexity and are easy to manufacture in bulk. They are suitable for various devices and applications from microcontrollers to power management ICs.

Ceramic Substrates: These are often made from materials like alumina or aluminum nitride. They offer high thermal conductivity, exceptional electrical insulation, robustness, reliability and can endure extreme environmental conditions, including elevated temperatures. Ceramic substrates are typically used in aerospace, automotive, and military applications where design reliability is critical.

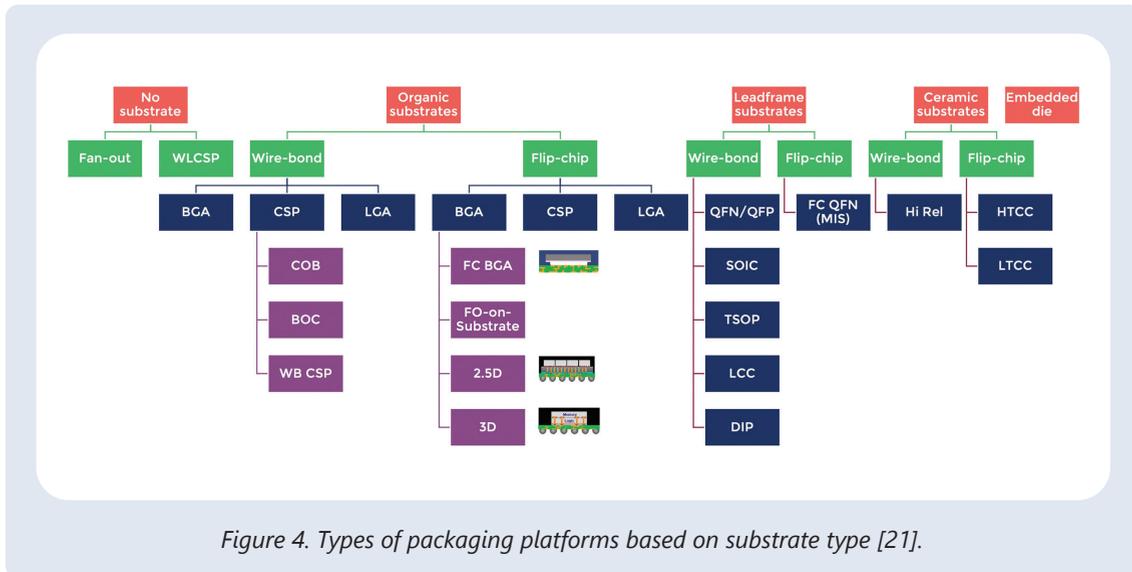


Figure 4. Types of packaging platforms based on substrate type [21].



Substrates are further classified by their distinct interconnect techniques, namely wire bond and flip chip technologies.

Wire Bonding (WB): Wire bonding is the traditional IC packaging method which provides versatility to suit various applications, is cost-effective for low to medium productions and has established reliability for processes and equipment. It is an interconnection process that uses a thin wire, heat, pressure, and ultrasonic energy in a welding process to create an electrical interconnection between the die and its carrier and, ultimately, the outside world (Figure 5). Wire bonding is classified based on the bonding type (ball bonding, wedge bonding, ribbon bonding, heavy wire bonding), type of input energy used for joining (thermocompression bonding, ultrasonic bonding, thermosonic bonding), and wire material (aluminum, copper, silver, gold). The major challenge for wire bonding technology is its scaling limitation in meeting density and performance requirements.

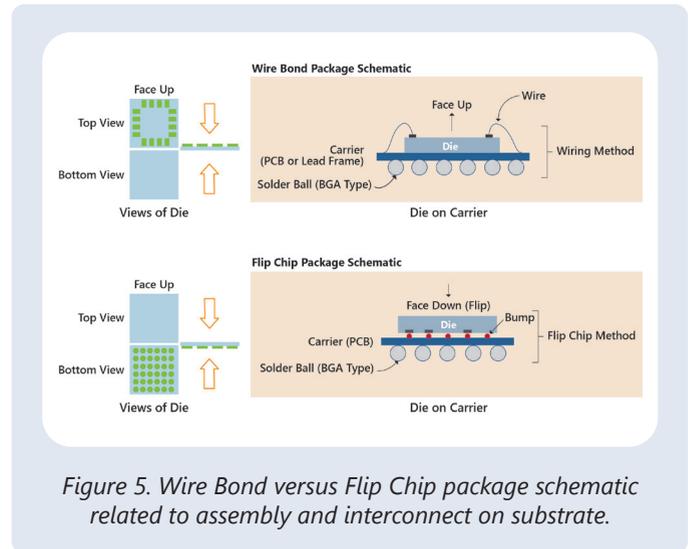


Figure 5. Wire Bond versus Flip Chip package schematic related to assembly and interconnect on substrate.

Flip Chip (FC): In the FC process, the die is placed directly on the substrate with the active surface at the bottom, without any further connecting wires i.e., the die is 'flipped' so that its top side faces down (Figure 5). In this process, solder "bumps" are first applied at electrical connection pads on the face of the chip. This allows for a higher pin count that can be achieved using wire bonding, reducing necessary die size, and optimizing signal integrity. Bump composition may be, for example, gold, a eutectic, lead, tin, or copper. The bumped die is flipped onto the substrate with its pads aligned with corresponding pads on the substrate, hence the name "flip chip." Bumps are bonded with the substrate pads by a variety of methods including thermosonic, and ultrasonic welding and thermocompression. Flip chip packages can be classified based on surface mount type that is employed, for example, Small Outline Integrated Circuit (SOIC), Small Outline Package (SOP), Quad Flat Pack (QFP), Plastic Leaded Chip Carrier, (PLCC), Ball Grid Array (BGA), Chip Scale Package (CSP) etc.

1.2.1.1 IC Packages with Substrates

Chip Scale Packages (CSP): A Chip Scale Package is a surface mountable integrated circuit (IC) package that has an area not more than 1.2 times the original die area. IPC's (Institute for Interconnecting and Packaging Electronic Circuits) standard J-STD-012 for Implementation of Flip Chip and Chip Scale Technology states that a chip must be a single-die and have a ball pitch of not more than 1 mm before it can qualify as a chip scale package. Chip scale packages are classified as:

- Customized leadframe based CSP (LFCSP)
- Flexible substrate based CSP
- Flip chip CSP (FCCSP)
- Rigid substrate based CSP
- Wafer level redistribution CSP (WL-CSP)



Ball Grid Array (BGA): A BGA package is a type of surface-mount packaging that employs an array of metal spheres called solder balls for electrical interconnection. The underside of the package is used for the connections, where solder balls are attached to a laminated substrate in a grid pattern. This substrate has conductive traces on the inside that connect the die-to-substrate bonds to the substrate-to-ball array bonds, using wire bonding or flip chip technology. Land Grid Array (LGA) and Pin Grid Array (PGA) are variations on this type of package (Figure 6). LGA packages use flat contact pads, or “lands,” on the bottom of the package. The corresponding contacts on the motherboard or socket interface with these lands establish electrical connections. PGA packages use pins protruding from the underside of the package, arranged in a grid pattern. These pins are inserted into corresponding sockets on the PCB.

Quad Flat Package (QFP): This package type is a surface-mount technology that has a square or rectangular form, with multiple electrical contacts located on the bottom surface. Unlike traditional leaded packages, the QFP does not have any leads extending from its sides. It may include a central exposed pad that serves as a thermal relief and an electrical ground. QFPs offer a blend of advantages, including a compact footprint, good thermal performance, cost-effectiveness, and robustness however, they can present severe thermal management and soldering complexity challenges.

High-Reliability (Hi-Rel) Ceramic Substrates: High-reliability ceramic substrates are typically made from alumina (aluminum oxide) or other ceramic materials and provide a rigid and thermally stable platform for mounting passive components and interconnects. They have excellent thermal conductivity and electrical insulation properties, making them ideal for use in high-power electronic modules, power amplifiers, microwave devices, and other applications that demand reliable operation in harsh environments.

Low-Temperature Co-Fired Ceramic (LTCC): These substrates are manufactured using a low-temperature (<1000°C) firing process and offer advantages such as high integration density, excellent RF/microwave performance, and the ability to create 3D structures within the package. Radiofrequency (RF), microwave applications, and sensors are the common uses for this substrate type.

High-Temperature Co-Fired Ceramic (HTCC): HTCC is similar to LTCC but is fired at much higher temperatures, often exceeding 1600°C. This high-temperature process allows for the use of specialized materials like alumina, aluminum nitride, or other ceramics that offer enhanced thermal and electrical properties. HTCC is preferred for applications where materials must withstand extreme temperatures, high power densities, and harsh operating conditions. This includes high-power semiconductors, automotive and aerospace electronics, and sensors for extreme environments.

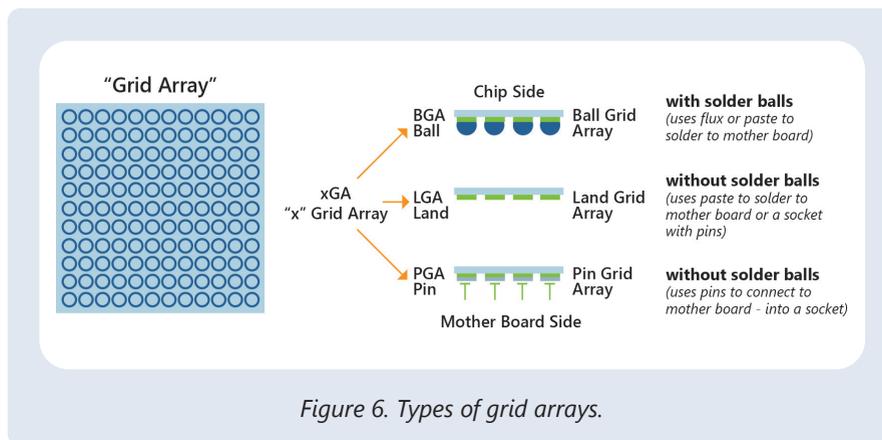


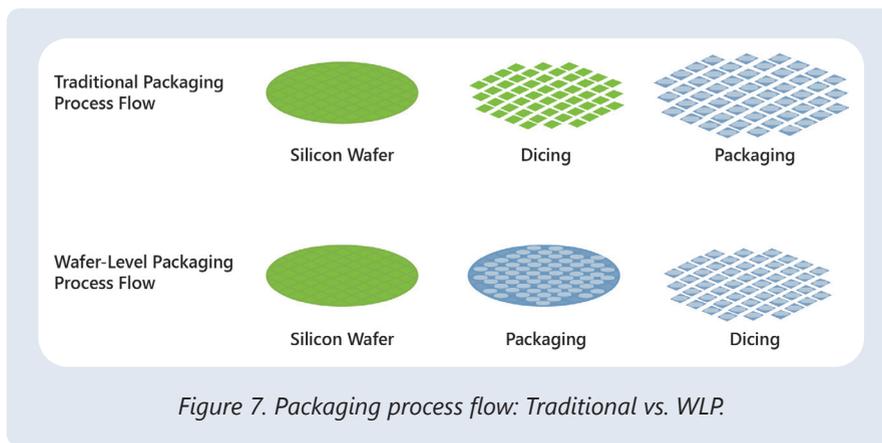
Figure 6. Types of grid arrays.



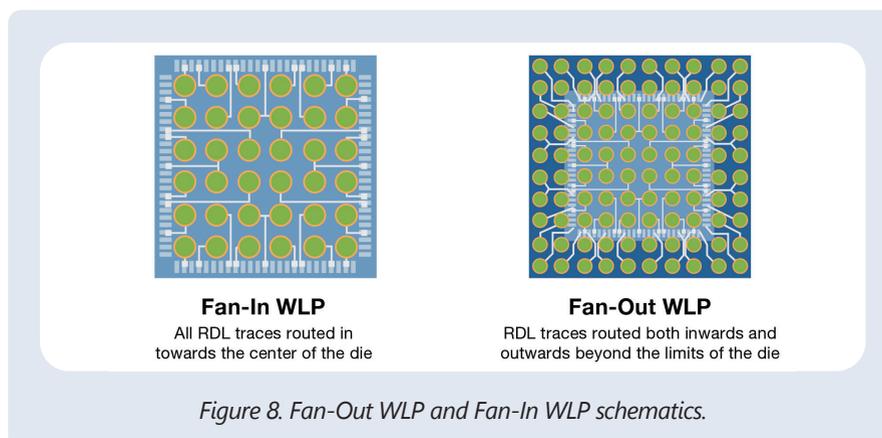
1.2.1.2 IC Packages without Substrates

Packages that do not employ a substrate use a production process that is referred to as Wafer Level Packaging (WLP). WLP packages the die while it is still on the wafer; that is, protective layers and electrical connections are added to the substrate before dicing. The sides of the die are not coated, resulting in a smaller size for the packaged chip which is obviously preferred for smaller device applications. WLP helps reduce manufacturing costs while allowing higher levels of integration. Figure 7 shows a comparison of WLP with conventional packaging process flow. WLP processes include:

Wafer Level Chip Scale Packaging (WLCSP): WLCSP is the smallest package currently available. It is just a bare die with a redistribution layer (RDL) to rearrange the pins or contacts on the die so they are big enough and have sufficient spacing to be managed. The advantage of WLCSP is not only its cost-to-performance ratio, but also its small die size—making it one of the most popular packaging techniques in the industry. However, its small size becomes a limiting factor for the number of inputs and outputs (I/O).



Fan-Out (FOWLP) and Fan-In Wafer Level Packaging (FIWLP): FOWLP and FIWLP enable increased functionality, low power consumption, and more I/O with smaller technology nodes and smaller dies. They allow stable or limited shrinkability in the I/O pitch while using standard PCBs in the next assembly level. The key difference between FOWLP and FIWLP is the size of the interposer relating to the die (Figure 8). An interposer is basically an electrical connection, and its purpose is to extend or reroute a connection. An interposer on a die in FIWLP is usually the same size as the die itself, whereas in FOWLP the interposer is larger than the die.





1.2.1.3 Embedded Die Substrates

Embedded die substrates embed the die directly within a PCB or a leadframe substrate during its formation process. The die is connected to other components on the substrate using copper-plated vias and conductive traces on the substrate surface [7]. This allows for significant reductions in electronic device package size.



1.3 Evolution in Packaging Architecture

The need for increased speed and reliability in electronic devices has produced important, but limited, innovations in IC packaging over the past few decades. The advent of flip chip packaging technology in the mid-90s was particularly important since it introduced a new paradigm for making interconnections between the semiconductor die and substrates. Following the introduction of flip chip, innovative approaches that further increase I/O counts, speed, and reliability in chip packages have evolved. In particular, the development of silicon interposer and Through Silicon Via (TSV) technology has enabled 2.5D and 3D heterogeneous integration in advanced device packaging. These approaches have facilitated dramatic advances in device size, I/O, speed, etc., but at the price of significant increases in manufacturing complexity and cost (Figure 9).

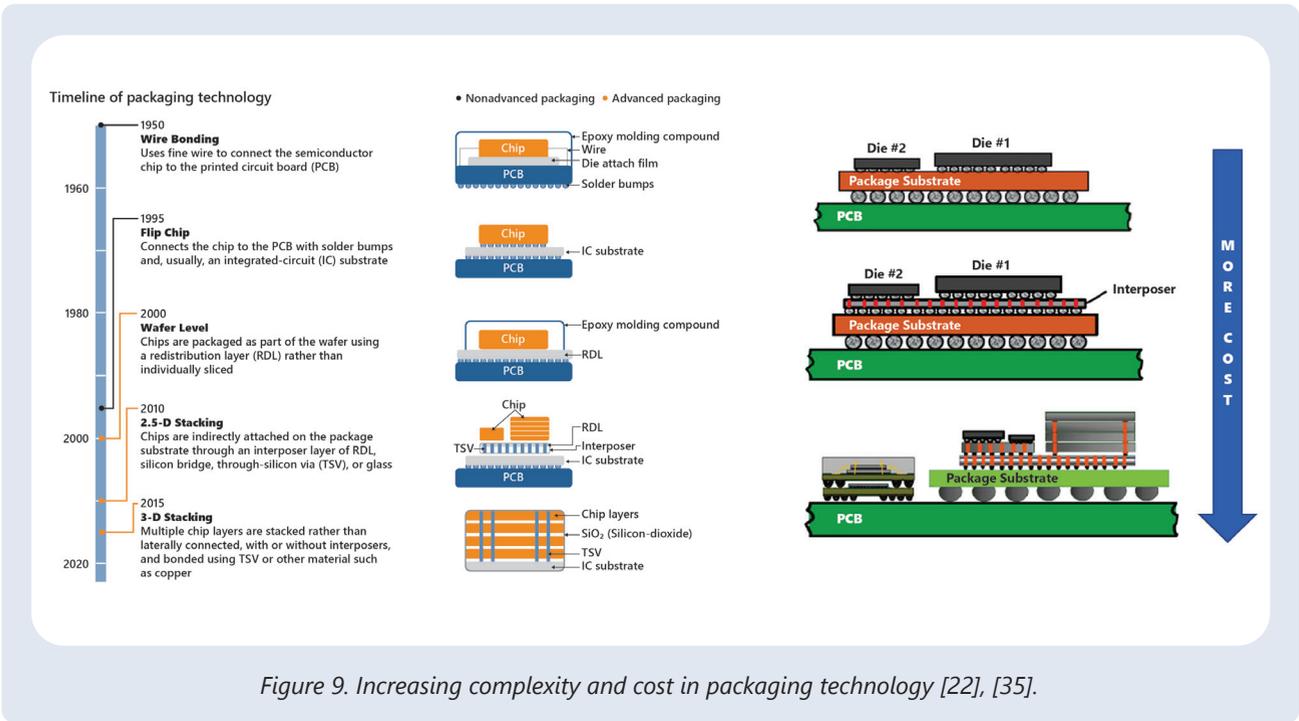


Figure 9. Increasing complexity and cost in packaging technology [22], [35].

Consequently, manufacturers continue to seek innovative interconnect bonding technologies that can reduce the cost of manufacture. For example, recent innovations in 3D integration use solder-free “bump-less direct bonding” interconnects between two die surfaces [8]. In a unique Thermal Compression Bonding (TCB) process, two die surfaces are joined so that the metal pad areas on each die are aligned. Once in contact, the TCB process is used to expand and join the die-to-die metal contacts to form an electrical connection while abutting dielectric surfaces on the two dies become bonded. This process has been labeled Hybrid Bonding. It is used extensively for device packages that employ chiplets to reduce the cost of manufacturing complex die. “Bump-less” interconnect technologies permit higher pitch scaling and reduce the cost of ownership compared to conventional bumping. Both Face-to-Face (F2F) and Face-to-Back (F2B) die orientations are supported, as described below. Figure 10 provides a schematic to assist in understanding the different terms used for advanced packaging schemes [9].

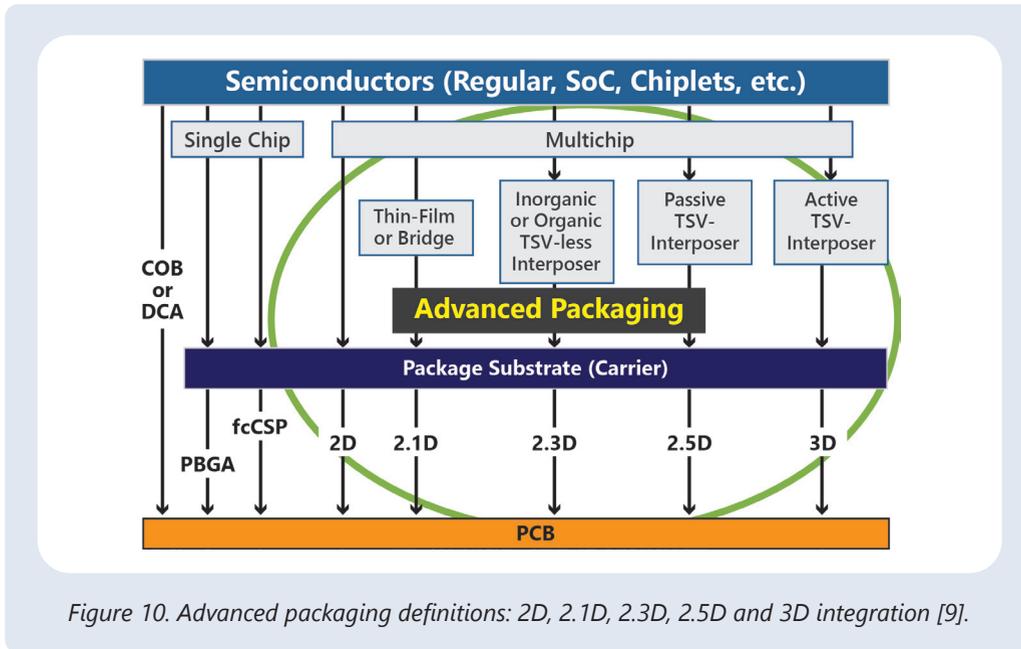


Figure 10. Advanced packaging definitions: 2D, 2.1D, 2.3D, 2.5D and 3D integration [9].



1.4 System-in-Package (SiP)

Packages that contain more than one chip and are designed to perform a specific task that can be a sub-task of a board, module or system, can be defined as a system-in-package (SiP). The development of SiPs is driven by application-specific requirements for the optimization of an intended function, e.g., mobile front-end / antenna modules, high performance computing chip sets, smart watch packages, etc. The availability of appropriate chipllets with needed functionality and integration capabilities are also factors that influence SiP design. There are many different SiPs available, each uniquely designed for a specific task.

The efficient connection of the various dies to each other and to the substrate is critical to the functioning of a SiP. While the most common interconnection processes remain wirebonding and Flip Chip (FC), continuing innovation has expanded the interconnection toolbox for SiP heterogeneous integration. Through Silicon Via (TSV), Through Mold Via (TMV), Through Glass Via (“TxV” in Figure 11) and Cu to Cu hybrid bonding have emerged as effective technologies for vertical interconnects. Innovations in horizontal or lateral interconnection, including redistribution layers embedded in dielectric interposers and embedded interconnect technologies such as the use of a silicon bridge die have facilitated the development of state-of-the-art SiPs.

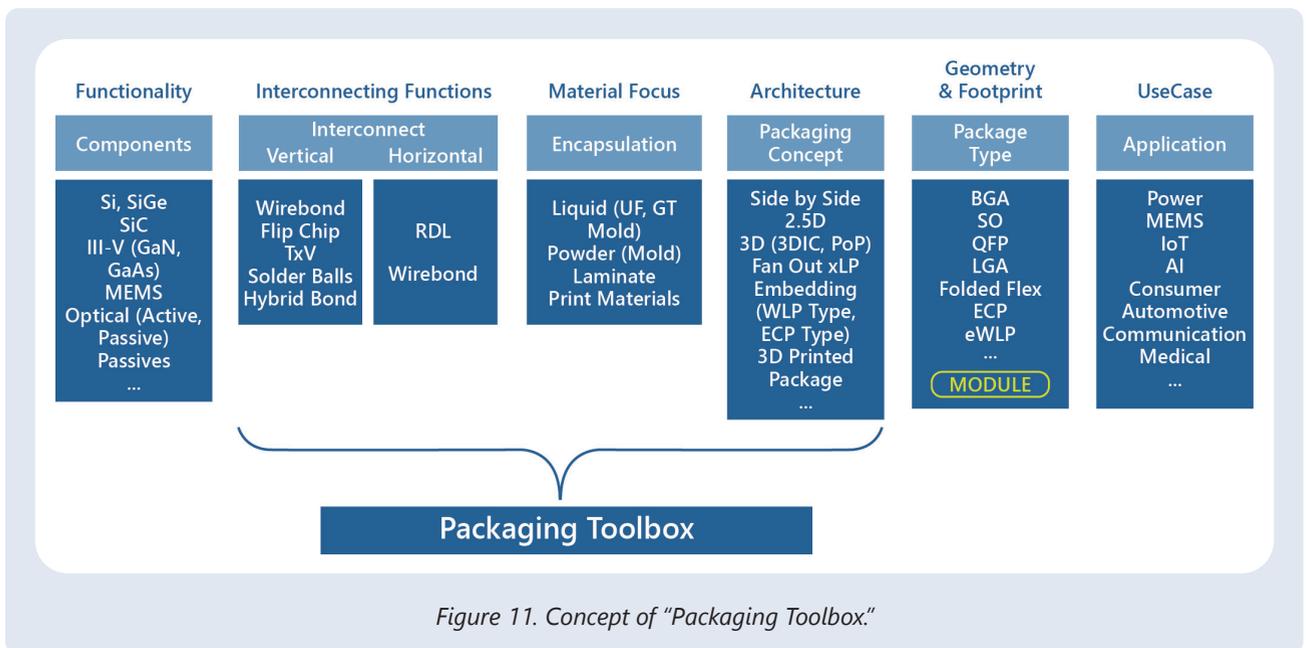


Figure 11. Concept of “Packaging Toolbox.”

1.4.1 SiP Modules

SiP modules are designed to enable complete system performance in a single small form factor unit in which several packaged components may be present. The level of integration can vary, but for the most complex systems such as smart phone and smart watch applications it is considerable, with RF components, MEMS, AP, memory, power, battery, display control and passive components all integrated onto a small HDI or SLPCB substrate (Figure 12). Packing density in these modules is very high, with die-to-die spacing typically in the one hundred microns or less range. Additionally, all real estate on both sides of the substrate is fully utilized to reduce the factor. In some mobile applications, a vertical



“donut” spacer containing vertical interconnects may be used to stack and connect two substrates with mounted components. Packaging concepts for the subcomponents in mobile applications (e.g., the low noise power amplifiers (PA), RF filters, front-end modules (FEM), and antennae) have changed dramatically as bandwidth requirements have increased. 5G cellular communication protocols, especially, have produced significant changes in packaging technology, as can be seen from the RF Packaging Roadmap compiled by Yole Development (Figure 13). The requirement for bandwidth increases at shorter wavelengths and higher frequencies produced a greater need for the low-loss integration of RF components, typically through the use of better dielectrics and shorter interconnects with improved trace smoothness. It is logical, therefore, to integrate all RF front end module components into a single SiP type package directly coupled to the Rx/Tx antenna to maximize performance.



Figure 12. Apple Watch Gen 3, an example module type SiP.

Due to the increased atmospheric signal attenuation at 5G transmission frequencies, antenna design has simultaneously undergone drastic changes. From the traditional omnidirectional dipole antenna in use for 4G and older communication protocols, there has been a shift towards integrating patch-based phased array antennas which allow transmission beam focusing and steering to reduce overall energy required for mobile communications at distance. Modern packaging concepts have allowed a fully integrated approach of moving patch antenna into the same module as the FEM components.

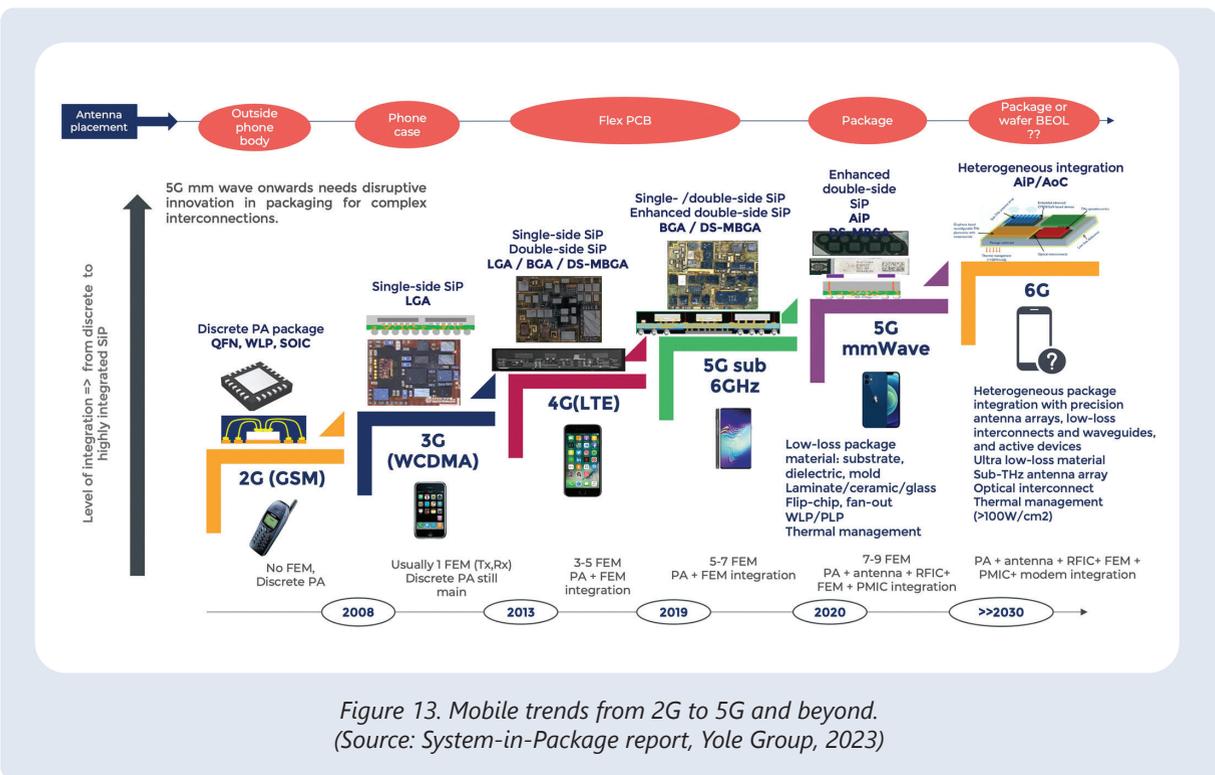
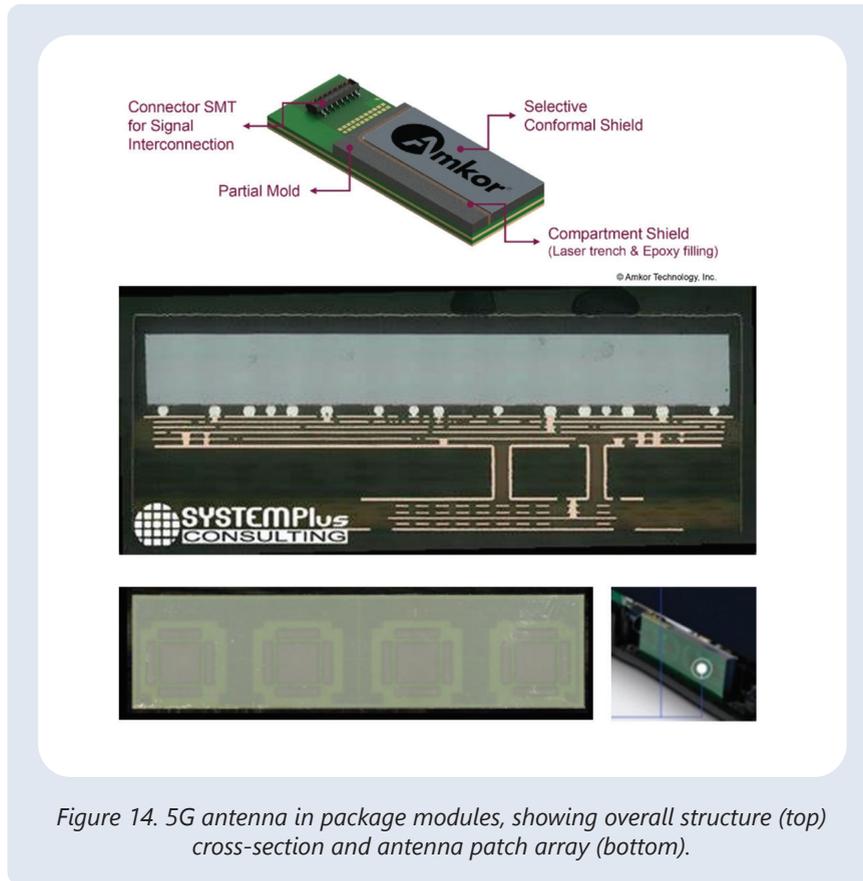


Figure 13. Mobile trends from 2G to 5G and beyond. (Source: System-in-Package report, Yole Group, 2023)



A fine example here is the QTM052 mobile RF/FE Antenna-in-Package (AiP) module from Qualcomm, manufactured by Amkor, an outsourced assembly and test provider (OSAT). This first-generation mobile RF/AiP module, designed for 5G, consists of a SiP containing several chips for signal processing, conditioning, and antenna control, all integrated into a single molded package as well as a patch array antenna made on the opposite side of the same laminate substrate (Figure 14) [36]. The use of Ajinomoto build-up film as the supporting build-up dielectric allows excellent low-loss signal processing. A typical 5G compatible handset will contain up to five of these modules to enhance connectivity as the phased array patch antenna typically has a limited transmission cone. Additionally, the signal can easily be blocked by obstacles like walls, foliage, and even hands which makes the case for improved connectivity through several modules placed at the mobile handset case periphery [37].

Other OSATs such as ASE, SPIL and IDM/Assembly giants such as TSMC and Samsung also provide their take on AiP. The integration with laminate substrate had been a typical OSAT approach whereas the IDMs such as TSMC were, from their inception, leveraging their fan-out wafer level packaging technologies. The Integrated Fan-Out Antenna in Package (InFO_AiP) approach from TSMC claims to improve on the laminate approach by selecting different dielectrics and embedding the RF components into a mold compound which reduces package thickness, shortens interconnect path lengths, decreases overall thermal resistance and improves overall signal quality. The Fan-Out AiP approach has been followed by many OSATs to date.



1.5 PCB and IC Substrate Fabrication and Packaging

A printed circuit board (PCB) is the foundation of most electronic devices. The PCB is the framework where all components are assembled to form an electronic device. It provides the electrical and mechanical support to the circuitry. Essentially, the PCB uses copper traces/pads and conductive planes to route the signals/power to the different components associated with the product. Today's PCBs integrate advanced packages, surface-mounted components, resistors, capacitors, various sensors, and antennas/amplifiers based on its application, making the PCB the backbone of most devices.

PCBs can have a varying degree of electrical and mechanical properties. These properties are determined by the properties of the materials used in their fabrication. These include dielectric properties, D_k and D_f , and CTE. Conductor thickness and length also play a critical role in signal integrity. Additional contributors are conductor roughness and the surface finish applied to the copper traces and the soldermask.

One of the key developments for the PCB has been the substrate materials the industry has accumulated in nearly a hundred years of history. The development of each stage of the substrate materials industry is driven by innovations in electronics, semiconductor manufacturing technology, electronic mounting technology, and electronic circuit manufacturing technology. Its development characteristics are mainly manifested in the resin, reinforcing materials, and insulating substrates. These have created the necessary conditions for the advent and development of the most typical substrate material for PCBs, the copper clad laminate.

There are different types of PCBs. The basic types are single layer (single sided) and double layer (double sided) which are ideal for simple electronic devices. Some PCBs are flexible, some are rigid. A flexible PCB enables the circuits to fold and bend into shape. Multi-layer PCBs are constructed with a core and built from alternating layers of conductive copper with layers of electrically insulating material. The number of layers in a PCB range from 1 to 40 layers with the multi-layer PCB being best suited for complex hardware.

While the industry continued to improve manufacturing processes for multilayer PCBs, high-density interconnect (HDI) PCBs arrived. Today, HDI PCBs are one of the fastest growing technologies in the PCB market. They contain blind and/or buried vias and often contain microvias of 60 - 70 micron or less in diameter. HDI has a higher interconnect circuitry density than traditional printed circuit boards. There are multiple types of HDI boards, through vias from surface to surface, with buried vias and through vias, two or more HDI layers with through vias and stacked vias, etc. By using HDI technology, designers now have the option to place more components on both sides of the raw PCB. Multiple via processes, including via-in-pad and blind via technology, allow for more PCB real estate to place components that are smaller, even closer together. Decreased component size and pitch allow for more I/O in smaller geometries. This means faster transmission of signals and a significant reduction in signal loss and crossing delays.

As the smartphone technology advanced from 3G to 4G LTE, the complexity of antenna configurations has made the RF front end take up more space in smartphones. In addition, the amount of data that needs to be processed has also grown enormously. So both of these needs have increased the number of components in a cell phone. Additionally, this has required an increase in battery capacity, which means that PCBs and other electronic components must be compressed. This has pushed HDI PCB toward thinner, smaller, and more complex processes achieving higher density and smaller form factor. A new printed circuit board, called Substrate-Like PCB (SL-PCB), was developed, reducing the volume of the mainboard by 30%, while all of the chips remained. The SL-PCB requires a more sophisticated manufacturing process, a modified Semi-Additive Process (mSAP), developed by PCB manufacturers and key supply chain partners such as Atotech. The more sophisticated manufacturing process allows for much finer line/space (L/S) dimensions to support the fine pitch BGA. Several years ago, 0.6 mm - 0.8 mm pitch



was applied in handheld devices. This generation of smartphones equips 0.4 - 0.3 mm pitch technology extensively due to the number of component I/Os and product miniaturization, which requires trace/spacing of 30/30 μm . The current HDI technology cannot meet this requirement any longer.

Originally, the IC substrate technology was developed from the HDI technology [38]. There is a certain correlation between both, but the technical threshold of an IC substrate board is much higher than an HDI or an ordinary multilayer PCB. Connecting the die and the printed circuit board, the IC substrate board is used as the middle interconnect. The IC substrate supports the routing of the die circuitry, with the PCB, and safeguards, supports, and reinforces the die, thereby giving it a thermal dissipation path. An IC substrate board can be seen as a high-end PCB, which has the characteristics of high density, high precision, high I/O, high performance, miniaturization, and thinness. It has higher requirements in a variety of technical parameters, especially the line width/line space parameter. Compared with ordinary PCB, there are many technical difficulties in IC substrate manufacturing.

A typical IC substrate is thin and easy to deform, especially when the thickness is less than 0.2 mm. To overcome this difficulty, breakthroughs have been made in plating thickness reduction, lamination parameters, and layer positioning systems to effectively control substrate warpage. In a word, an IC substrate PCB has more requirements than standard PCB and HDI PCB. The barriers of the IC substrate industry are high, not limited to the technical threshold. High technical requirements and numerous patent restrictions have created a high threshold of the IC substrate industry, and the barriers within the industry also include capital and manufacturers.

The verification system for an IC substrate manufacturer is stricter than for a PCB manufacturer, in relation to both the quality of the die and the PCB connection. Industry generally adopts the "qualified supplier system". This requires suppliers to have a sound operation network, efficient information management system, rich industry experience, good brand reputation, and the ability to pass strict certification procedures. IC Packaging substrate is the largest cost of IC packaging, accounting for more than 30%. The cost of IC packaging includes packaging substrate, packaging materials, equipment depreciation, and testing. Shown in Figure 15, the substrate landscape from the PCB to semiconductor is changing. The call for high IO/mm² density, increased computer processing, and larger silicon die, drives the advanced packaging industry. So, the substrate landscape is being pushed for shrinkage of lines and space, and to keep costs at a minimum. However, this shift is not simple and clearly requires considerable shift in technology, manufacturing methodologies, and capital investments. At the same time the substrate manufacturers must maintain process yield and reliability which becomes challenging.

Advancements of the substrate technologies cannot be kept in line with semiconductor technologies' advancements, as the resources and capital spend on substrate development is a fraction of those of the semiconductor industry. This gap is decreasing but at a very slow rate. Ultimately, it comes down to the total cost of the device. Cost also has to meet the expectations of the customer, so this gap will remain and the use of glass core technology in the IC substrate will help shrink this gap in the near future.

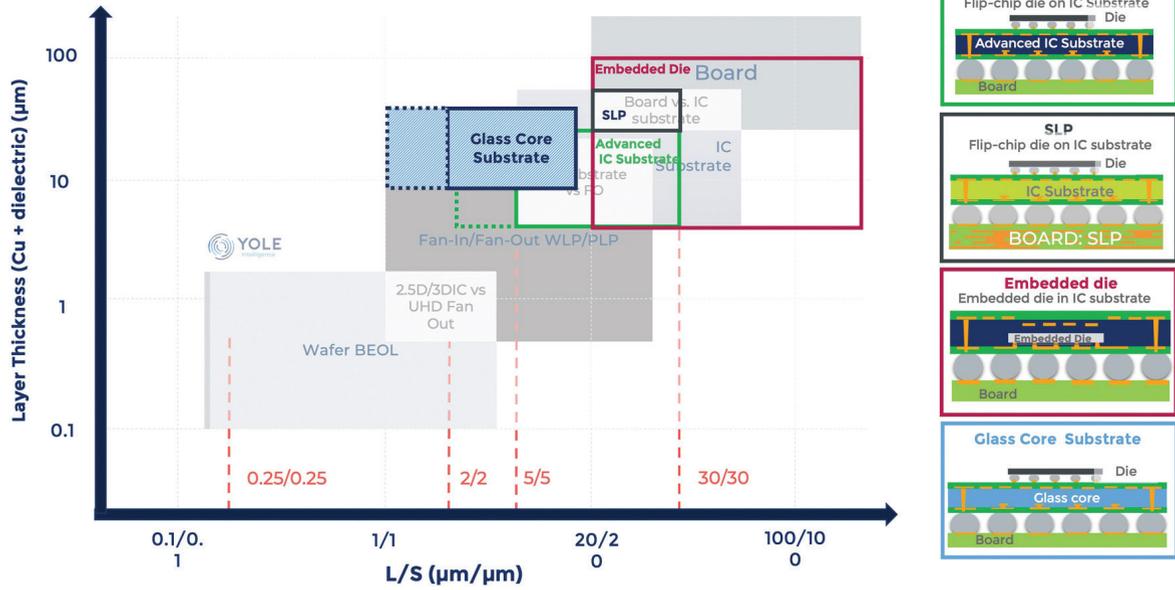


Figure 15. Substrate landscape showing the relationship of lines/space and layer thickness. (Source: Status of the Advanced IC Substrate report, Yole Group, 2024)

1.6 Technology Roadmaps

The first U.S. National Technology Roadmaps for Semiconductor (NTRS™) were developed in the late 1980s by SEMATECH, a consortium between government and the U.S.-based semiconductor industry, formed in Austin, TX in 1987. The first NTRS report was produced in 1994 followed by a revision in 1997. By 1998, the U.S., European, and Asian semiconductor industries had become much closer and an industry-wide team of experts from Europe, Japan, Korea, Taiwan, and the US began to collaborate on producing an International Technology Roadmap for Semiconductors (ITRS™). Beginning in 2001, the ITRS underwent nine revisions, the last published in 2015. It served as the main reference for development efforts in various areas of semiconductor device technology for university, consortia, and industry researchers. Recently, it has become clear that the industry is moving beyond conventional CMOS device technology. Consequently the semiconductor industry has reorganized its approach to these technology roadmaps. The Semiconductor Research Corporation has published the “2030 Decadal Plan for Semiconductors” [10] in 2020 with the goal to “outline(s) research priorities in information processing, sensing, communication, storage, and security.” SRC extended this work in 2023 with the release of the “Microelectronics and Advanced Packaging Technologies Roadmap” (SRC-MAPT) [5].

The Institute of Electrical Electronics Engineers (IEEE) recently released an extension of the NTRS/ITRS that takes a more systems-oriented approach to a roadmap for future electronic devices. This “International Roadmap for Devices and Systems” (IRDS™) has the stated mission: “To identify the roadmap of the electronic industry from devices to systems and from systems to devices”. This broad approach spans topics from devices to systems and from systems to devices, “in which the AI-centric IoT-social-infrastructures with high-speed network communication will be built on the semiconductor device and process technologies” [11]. It is intended to encourage innovation using non-traditional paradigms for system development and to encompass a broad scope of development directions for future electronic devices and systems (Figure 16).

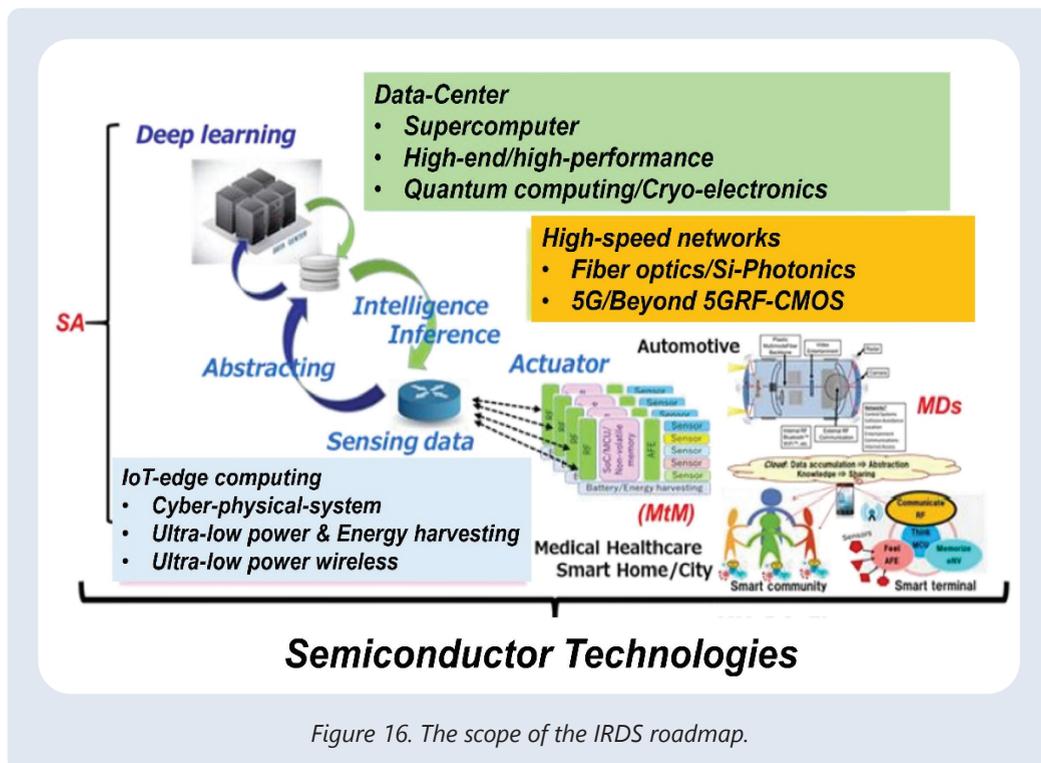


Figure 16. The scope of the IRDS roadmap.



This shift and evolution of the roadmap from the ITRS to the IRDS has translated to an expanded focus on systems. The IDRS has the following goals [11]:

To identify key trends related to devices, systems, and all related technologies by generating a roadmap with a 15-year horizon.

To determine generic devices' and systems' needs, challenges, potential solutions, and opportunities for innovation.

To encourage related activities worldwide through collaborative events, such as related IEEE conferences and roadmap workshops.

The foreseeable technological innovations needed in future computing and sensing applications have been outlined in the SRC-MAPT and IRDS reports. Semiconductor packaging will evolve to include a range of technologies such as 2.5D/3D heterogeneous integration, chiplets, FOWLP, and SiP. Each of these offers an array of options for assembling and integrating complex dies in an advanced package, providing die customers with many possible ways to differentiate their new IC designs. The SRC-MAPT report especially emphasizes the need for intimate coordination throughout the design cycle for application-specific chiplet and packaging combinations (Figure 17). System architects must be involved in all phases of the design process to “analyze the system and packages, partition the design into various chiplets, and assess necessary tradeoffs in computing data movement and fabrication costs” [5]. This means that the relevant aspects of the packaging design must be considered during each step of the design cycle. This is a very different approach to the current one in which ASIC and package design phases are separate activities. Within this approach, there are many possible configurations, making design choices for a particular application very challenging even for the most sophisticated design teams. HI system designs will have to pay special attention to challenges in timing analysis for the chiplet-to-chiplet interface, thermal/mechanical stress analyses, and power delivery and integrity [5]. Intel, AMD, Arm, and all three leading-edge foundries are currently involved in the joint development of a new open standard for chiplet interconnects which is named Universal Chiplet Interconnect Express, or UCIe. The UCIe will enable very fine pitch I/O and L/S circuitry for chiplet interconnects. This new standard will facilitate the achievement of the fundamental performance requirements of higher bandwidth and efficiency in future electronic devices.

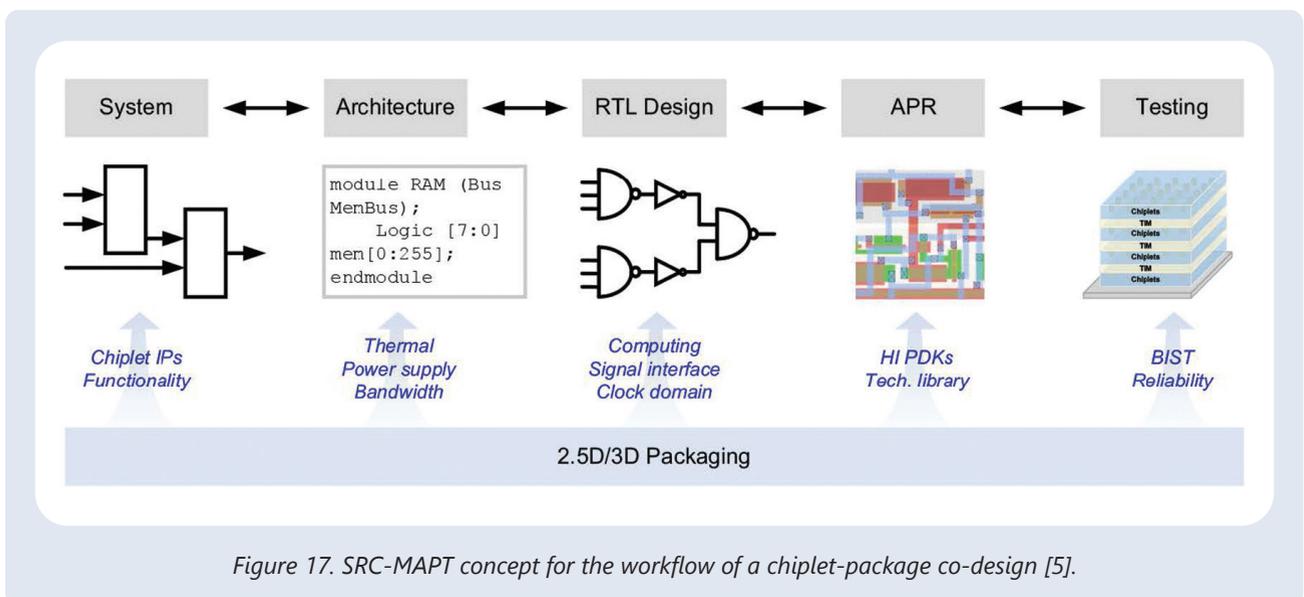


Figure 17. SRC-MAPT concept for the workflow of a chiplet-package co-design [5].



Advanced packaging concerns are thus playing a bigger role across the semiconductor industry. Networking equipment, servers, smartphones and even watches are among the applications that are adopting advanced packaging approaches. While not all chips require advanced packages and most chips are assembled and housed in mature and commodity packages, even for these products, IC vendors still seek new packages with smaller form factors and better electrical performance.



References

- [1] A.-S. Lesiv, *Foundation & Frontiers, The Evolution of Chips*.
- [2] NXP, "NXP Semiconductors: IC Packages," [Online]. Available: <https://www.nxp.com/products/nxp-product-information/packages:IC-PACKAGES>.
- [3] IEEE Electronics Packaging Society, "Heterogeneous Integration Roadmap 2023 Edition," IEEE Electronics Packaging Society, 2023. [Online]. Available: <https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2023-edition.html>.
- [4] The White House, "The White House 100-Day Review, "Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Base Growth," US Government, Washington, DC, 2021.
- [5] Semiconductor Research Corporation, "Microelectronics and Advanced Packaging Technologies Roadmap," Semiconductor Research Corporation, 2023.
- [6] W. T. Chen, "The Future Is Heterogeneous Integration," [Online]. Available: <https://www.3dincites.com/2021/01/the-future-is-heterogeneous-integration/>.
- [7] ASE Technology Holding, "Embedded Die Substrate," ASE Technology Holding, 2023. [Online]. Available: <https://ase.aseglobal.com/embedded-die/>.
- [8] A. Roshanghias, J. Kaczynski, A. Rodrigues, R. Karami, M. Pires, J. Burgraaf and A. Schmidt, "3D Integration via D2D Bump-Less Cu Bonding with Protruded and Recessed Topographies," *ECS Journal of Solid State Science and Technology*, vol. 12, p. 084001, 2023.
- [9] J. H. Lau, "Recent Advances And Trends In Advanced Packaging," *IEEE.TV*, 2022. [Online]. Available: <https://ieeetv.ieee.org/video/recent-advances-and-trends-in-advanced-packaging>.
- [10] Semiconductor Research Corporation, "2030 Decadal Plan for Semiconductors," Semiconductor Research Corporation, 2020.
- [11] Institute of Electrical Electronics Engineers, "International Roadmap for Devices and Systems™," IEEE, 2023. [Online]. Available: <https://irds.ieee.org/>.
- [12] Y. Nishi and R. Doering, *Handbook of Semiconductor Manufacturing Technology*.
- [13] "SemiWiki: Package Technologies Evolution," [Online].
- [14] M. & Company, "Advanced chip packaging: How manufacturers can play to win," [Online]. Available: <https://www.mckinsey.com/industries/semiconductors/our-insights/advanced-chip-packaging-how-manufacturers-can-play-to-win>.
- [15] S. Choi, C. Thomas and F. Weig, "Advanced-packaging technologies: The implications for first movers and fast followers," McKinsey & Co., [Online]. Available: https://www.mckinsey.com/~media/mckinsey/dotcom/client_service/semiconductors/issue%20%20autumn%202014/pdfs/mosc2014_advanced-packaging_technologies_the_implications_for_first_movers_and_fast_followers.ashx.
- [16] S. Liu, . K.-N. Chen and T.-Y. Tsai, in *Semiconductor Packaging: A Multidisciplinary Approach*, A. Kraus, H. R. and P. M. , Eds., New York, NY: John Wiley & Sons, 1994.
- [17] Y. Development, "High-End Performance Packaging: 3D/2.5D Integration Yole Report 2022," Yole Development, 2022. [Online]. Available: <https://s3.i-micronews.com/uploads/2022/03/High-End-Performance-Packaging-2022-Product-Brochure.pdf>.



**CLICK HERE TO
DOWNLOAD
THE FULL
BOOK**

- [18] R. R. Tummala, E. J. Rymaszewski and A. G. Klopfenstein, *Technology Drivers Part 1*, New York: Springer, 1997.
- [19] D. C. Brock, A. Thakray and R. Jones, "How Gordon Moore made (Backchannel)", 16 April 2015.
- [20] G. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, 38, no. 8, 19 April 1965.
- [21] Yole Group, "Status of the Advanced Packaging Industry report," 2024.
- [22] O. Burkacky, T. Kim and I. Yeom, "Advanced Chip Packaging," McKinsey & Company.
- [23] A. Chen and R. Hsiao-Yu Lo, *Semiconductor Packaging: Materials Interaction and Reliability*, Boca Raton, FL: CRC Press Taylor & Francis Group, 2017.
- [24] N. Shimizu and et al, "Development of Organic Multi Chip Package for High Performance Application," in 46th International Symposium on Microelectronics (IMAPS 2013) | , Orlando, FL USA, 2013.
- [25] A. Usman and e. al, "Interposer Technologies for High Performance Applications," *IEEE Trans. on Components, Packaging, and Manufacturing Technology*, p. 99, 2017.
- [26] H. Tameda and et al, "2.3D," in 28th MES Autumn Meeting Mission Fellow, Osaka University, Japan, 2018.
- [27] H. H. Utsunomiya, "Latest Topics of 2.1/2.5D IC Integration and Challenges," in PanPac, Kauai, HI, USA, 2015.
- [28] IBE Electronics, "2.5D Package," IBE Electronics, 2022. [Online]. Available: <https://www.pcbaaa.com/advanced-packaging/#2.5D-package>.
- [29] C.-F. Tseng, C.-S. Liu, C.-H. Wu and D. Yu, "InFO (Wafer Level Integrated Fan-Out) Technology," in IEEE 66th Electronic Components and Technology Conference, Las Vegas, NV, USA, 2016.
- [30] Samsung, "Samsung Electronics Announces Availability of Its Next Generation 2.5D Integration Solution '1-Cube4' for High-Performance Applications," Samsung, 2023. [Online]. Available: <https://semiconductor.samsung.com/news-events/news/samsung-electronics-announces-availability-of-its-next-generation-2-5d-integration-solution-i-cube4-for-high-performance-application/>.
- [31] E. Sperl, "Advanced Packaging Confusion," *Semiconductor Engineering*, 13 June 2018. [Online]. Available: <https://semiengineering.com/advanced-packaging-confusion/>.
- [32] IEEE Electronics Packaging Society, "Heterogeneous Integration Roadmap Chapter 22: Interconnects for 2D and 3D Architectures," 2021.
- [33] Yole Development.
- [34] IEEE Electronics Packaging Society, "Definitions," IEEE Electronics Packaging Society, 2024. [Online]. Available: <https://eps.ieee.org/technology/definitions.html>.
- [35] <https://nepp.nasa.gov/docs/etw/2018/19JUNE18/1330a%20-%20Sheldon%20-%20NEPP%20ETW%20djs%20final.pdf>.
- [36] <https://www.techinsights.com/blog/qualcomm-qtm052-mmwave-antenna-module>
- [37] <https://www.yolegroup.com/product/report/qualcomms-first-5g-mmwave-chipset-sdx50m-and-qtm052/>
- [38] www.rocket-pcb.com/blog/IC-substrate-technology-guide